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Through Silicon Via (TSV) Process Using DRIE and Cathode Coupled PE-CVD

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1. Introduction

The TSV process is central to realization of further miniaturization and density improvements in 3D LSI. We have developed solutions for deep silicon etching using the Bosch process (1), and sidewall insulating film deposition using cathode-coupled liquid-source PE-CVD for via-last applications (2). Specifically, SAMCO's cathode coupled PE-CVD systems (PD-270STLC for 200mm and PD-330STC for 300mm) feature proprietary technology allowing the deposition of sidewall insulator films with excellent sidewall coverage.

2. Experimental

Via hole etching was carried out by the SAMCO RIE-800iPB DRIE system using SF_6 and C_4F_8 gases. The Bosch process consists of alternating cycles of isotropic etching using SF_6 and passivation layer deposition using C_4F_8.

Sidewall insulator film deposition was carried out at 80ºC by the SAMCO PD-270STL cathode coupled PE-CVD system using TEOS (Tetra Ethyl Ortho Silicate) and oxygen. In cathode coupled PE-CVD, positive ions in the plasma are attracted toward the negatively-biased wafer electrode. In RF driven plasmas, an ion sheath is formed near the lower electrode. Positive ions from the sheath are accelerated vertically to the negatively charged electrode and using the kinetic energy of the ions. High quality silicon dioxide can now be deposited at low temperature and at high rates.

3. Results

In Fig.1(a) a ϕ50µm wide, 125µm deep (aspect ratio of 2.5:1) hole was formed at an etch rate of 10µm/min and uniformity of ±2.5% (200mm). In Fig.1(b) holes ϕ5µm wide and 50µm deep (aspect ratio of 10:1) were formed with minimized scalloping at an etching rate of 2µm/min.

In Fig.2 sidewall insulating film was deposited into a 50µm wide, 100µm deep hole (aspect ratio of 2:1). The thickness ratio of the oxide film on the upper-sidewall, lower-sidewall, and hole bottom was 0.43, 0.29, and 0.4 of the surface film thickness, resulting in excellent electrical insulation. Breakdown voltage at the top was 7MV/cm.

For researchers and customers demanding higher aspect ratio deposition, 100% coverage of 6µm wide, 120µm deep holes (aspect ratio of 20:1) has been achieved using cathode coupled PE-CVD. The thickness ratio of the oxide film on the sidewalls, and hole bottom was 0.067 and 0.083 of the surface film thickness.

4. Conclusion

Both via hole etching and film deposition was carried out with excellent coverage and breakdown voltage using DRIE and cathode coupled PE-CVD. We believe that this technology is effective for the fabrication of 3D LSI.

(1)N. Kuratomi, *et al.*, Microelec. Assem. Pack., Fukuoka, Japan, (2010) p.13.
(2)Y. Kusuda, *et al.*, Microelec. Assem. Pack., Fukuoka, Japan, (2009) p.41.

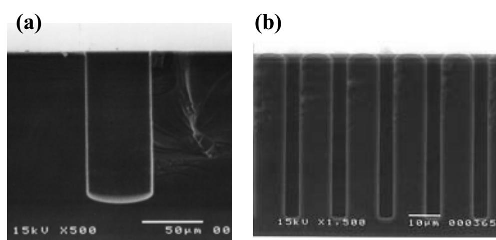
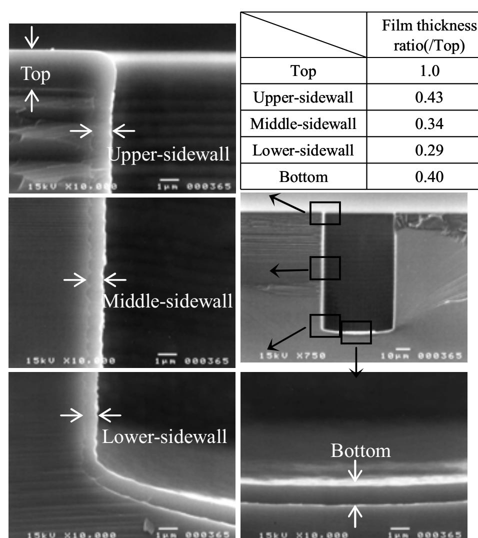


Fig.1 Via hole etching using the Bosch process. (a)aspect ratio 2.5:1 (b)aspect ratio 10:1



	Film thickness ratio(/Top)
Top	1.0
Upper-sidewall	0.43
Middle-sidewall	0.34
Lower-sidewall	0.29
Bottom	0.40

Fig.2 Coverage of the via hole using cathode coupled PE-CVD. (aspect ratio 2:1)

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