

# Stable Device Isolation Processing for 6-Inch GaN-Based Power Devices

## Introduction

Gallium nitride (GaN)-based semiconductors are anticipated to serve as next-generation power device materials to replace silicon (Si). Owing to their superior physical properties, such as a wide bandgap and high electron mobility, GaN-based semiconductors have been extensively researched and developed, along with silicon carbide (SiC)<sup>1</sup>. These materials have already been commercialized in high-frequency devices for signal amplification, as well as in power devices for power control and conversion, and their market continues to expand<sup>2</sup>.

In particular, GaN high-electron-mobility transistors (GaN-HEMTs), which require low ON-resistance and high channel mobility, have been successfully fabricated on Si substrates<sup>3</sup>. As a result, production using 6-inch and 8-inch wafers is now underway. Samco Inc. supplies ICP-RIE and CVD systems for fabricating GaN-based light-emitting devices, which are widely used from research and development through mass-production processes. The etching rate, in-plane uniformity, and stability

during continuous processing of Samco's ICP-RIE systems have been highly evaluated by many users.

In this report, continuous device isolation processing of GaN-based power devices formed on 6-inch Si substrates was investigated using the mass-production-ready ICP-RIE system RIE-800iPC. The stability of continuous processing for 25 wafers is reported.

## Experimental Procedure

Device isolation etching was performed on a cassette of 25 6-inch Si wafers with a GaN layer using the ICP-RIE system RIE-800iPC to evaluate the stability of a mass-production process. Figure 1 shows the external appearance of the RIE-800iPC. The etched sample structure is shown in Figure 2. A GaN layer with a thickness of approximately 7 μm was formed on a Si substrate, and a photoresist (PR) mask was patterned through exposure and development. The patterned PR mask covered approximately 90% of the wafer, leaving an opening area of about 10%.

Device isolation processing requires etching the GaN layer down to the Si substrate, and this condition must be achieved uniformly across the entire

6-inch wafer. Consequently, some over-etching into the Si substrate is inevitable. Excessive over-etching, however, may cause device damage and height non-uniformity, leading to reduced accuracy in subsequent processes. In addition, variations in GaN layer thickness exist between wafers.

To stabilize the over-etching amount, an optical emission spectroscopy-based endpoint monitor (HORIBA EV-140C) was employed.

## Experimental Results

Continuous processing of 25 wafers loaded into a single cassette was performed using endpoint detection. The GaN layer thickness of the wafers used in this experiment was approximately 7 μm, with thickness variations of several percent among the wafers. Since etching was performed until the Si substrate was reached based on the endpoint detection recipe, stable etching rates yield etching times that correspond to the GaN film thickness of each wafer.

Figure 3 presents the endpoint detection result and cross-sectional scanning electron microscope (SEM) images at the wafer center for the first wafer in the 25-wafer continuous process, in which over-etching was controlled by automatic etch stop based on endpoint detection. In the endpoint detection graph, the green line represents the emission intensity of nitrogen (N), and the red line represents that of silicon (Si). After completion of GaN etching, the Si emission intensity increased, and the etching was stopped at 648 s when the signal stabilized. Cross-sectional



Figure 1. ICP-RIE system RIE-800iPC

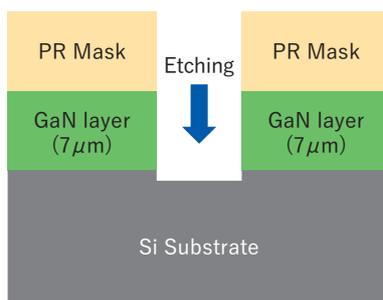


Figure 2. Sample structure and GaN layer etching using a PR mask

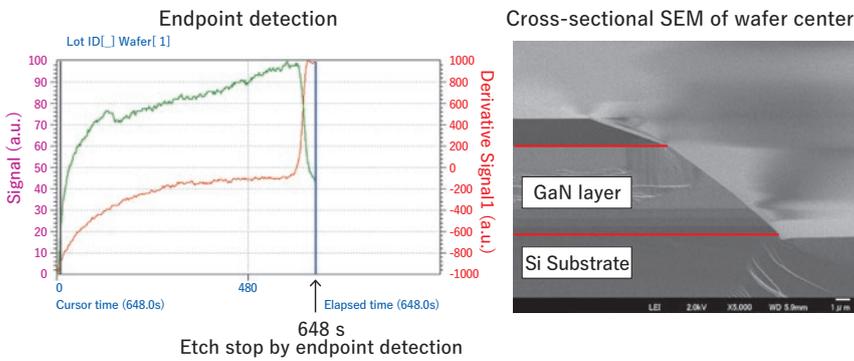


Figure 3. Etch stop based on endpoint detection and cross-sectional SEM results for the first wafer in 25-wafer continuous processing

SEM observation confirmed that the GaN layer had been completely etched and that the Si substrate had been reached.

To evaluate within wafer etch uniformity and etching rate stability, the 1st, 13th, and 25th wafers were selected from the lot. Etch depth measurements were conducted using a stylus profilometer, and etching rates were calculated from the etching time. The results are shown in Figure 4.

For the three wafers (1st, 13th, and 25th), step height measurements were performed at nine points excluding the outer 5 mm edge region. The average etching rate was 675 nm/min, within wafer uniformity was  $\leq \pm 3\%$ , and the etching rate uniformity within the lot was  $\pm 0.35\%$ . These results confirm the stability of the process during

continuous processing of 25 wafers.

Finally, the etch stop times for all 25 wafers are shown in Figure 5. The etch stop times ranged from 641 to 670 s, corresponding to a variation of  $\pm 2.2\%$ . Given that the etching rate variation was only  $\pm 0.35\%$ , this indicates that the variation in etch stop time is primarily due to differences in GaN film thickness between wafers. These results demonstrate the effectiveness of endpoint monitoring in controlling the over-etching amount, even for wafers with several-percent differences in GaN film thickness.

### Conclusion

This report has presented a device isolation processing technique for GaN-based power devices using

the mass-production-ready ICP-RIE system RIE-800iPC, along with its excellent process stability. Featuring high process reproducibility and superior in-plane etch uniformity, the RIE-800iPC is suitable not only for GaN semiconductor etching but also for a wide range of materials, including compound semiconductors such as GaAs and InP, and Si-based materials such as SiO<sub>2</sub> and SiN. It also supports ferroelectric and metallic materials such as PZT and Pt, as well as polymer materials such as polyimide.

Samco will continue to actively promote the development of process technologies for next-generation devices, contributing to resolving stability issues and improving quality in customers' mass-production processes.

### References

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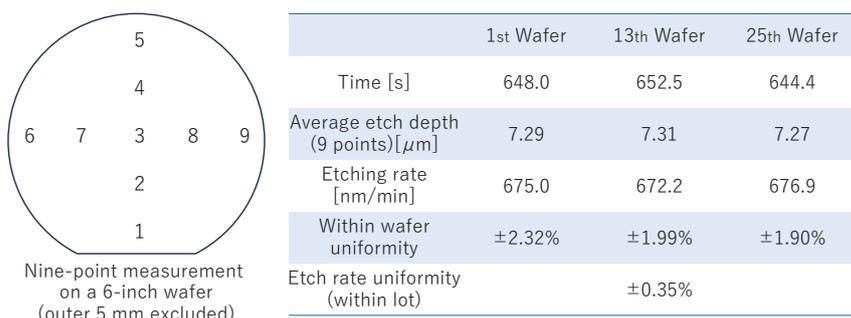


Figure 4. Within wafer uniformity and etching rate results for the 1st, 13th, and 25th wafers

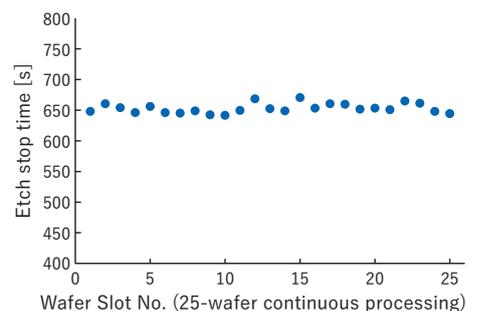


Figure 5. Etch stop times during 25-wafer continuous processing