



deposition



etching



surface
treatment

Next-generation GaAs VCSEL Plasma Etch Process Technology

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Next-generation GaAs VCSEL

Plasma Etch Process Technology

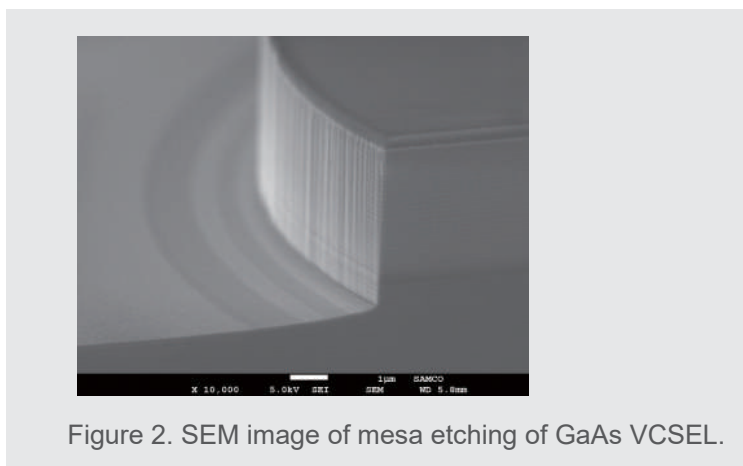
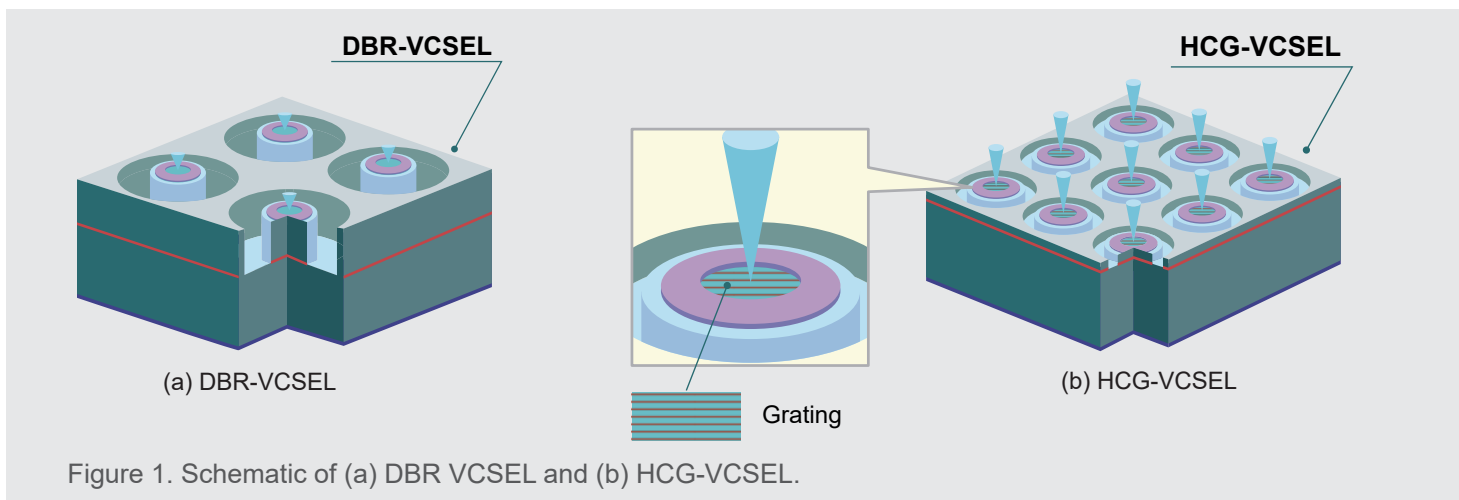
Introduction

The market for Vertical Cavity Surface Emitting Lasers (VCSEL), which were invented in 1977 by Professor Iga of Tokyo Institute of Technology, has been expanding in recent years for optical communication and sensor applications. The production process of VCSELs requires plasma etching and plasma enhanced CVD equipment, and our products are used by many users worldwide from research and development to mass production. This paper introduces the latest plasma etching process examples of VCSEL on our ICP etching system RIE-400iP.

GaAs VCSEL Mesa Etching

Figure 1 (a) shows a typical VCSEL structure currently on the market. Completing a VCSEL device requires multiple plasma etch processes such as mesa etching and element separation etching. Mesa etching is the process of etching the multi-layer film reflector (DBR; Distributed Bragg Reflector) and the active layer.

Figure 2 shows an example of vertical mesa etch processing on a $\phi 3$ inch wafer. The etch rate was 320 nm / min and the selectivity to the silicon nitride mask was 25:1. By observing the clear DBR contrast, it is known that the etched side wall is very smooth.



ICP Etch System RIE-400iP

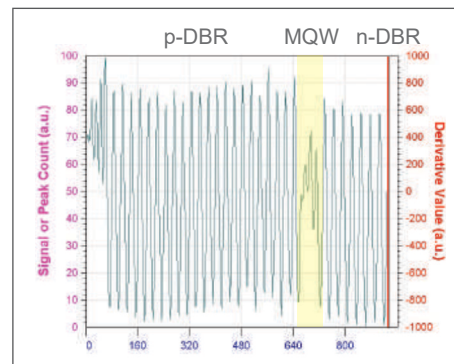


Figure 3 shows the interference reflection and emission spectroscopy endpoint waveforms acquired during the etching. Both waveforms can detect DBR and active layer, and the etching can be stopped at the target depth. Endpoint detectors are effective in improving the quality of VCSEL wafers.

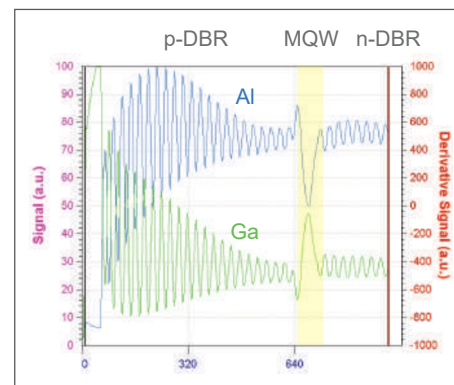
We have developed an etch process technology that enables high-speed vertical machining up to and including $\phi 6$ inch wafers. Figure 4 shows an example of a GaAs mesa etching process with an etching rate of about $2 \mu\text{m} / \text{min}$. A selectivity of about 18:1 to resist masks and 70:1 to silicon nitride masks have been achieved.

Etching of GaAs HCG-VCSEL

By replacing the upper DBR of the active layer with a diffraction grating, it is possible to improve the performance of the VCSEL. Figure 1 (b) is a high-refractive index sub-wavelength diffraction grating (HCG) -VCSEL, and is attracting attention as a next-generation VCSEL that not only thins the epi layer but also has a polarization control function.¹⁾ Figure 5 shows an example of HCG processing of a $\phi 6$ inch GaAs wafer patterned with a resist mask with an etch depth of 340 nm and GaAs (275 nm) / Air-gap (190 nm) intervals. The etch rate was about 50 nm / min, and the selectivity to a resist mask was about 5:1. A vertical and smooth side wall was obtained, and the $\phi 6$ inch in-plane uniformity was very good at 3.3%.



(a) Interference reflection endpoint waveform



(b) Optical emission spectroscopy endpoint waveform

Figure 3. In-situ monitoring of GaAs DBR VCSEL etching. (a) Interference reflection endpoint waveform and (b) optical emission spectroscopy endpoint waveform.

Both high rate and nano etch process are feasible

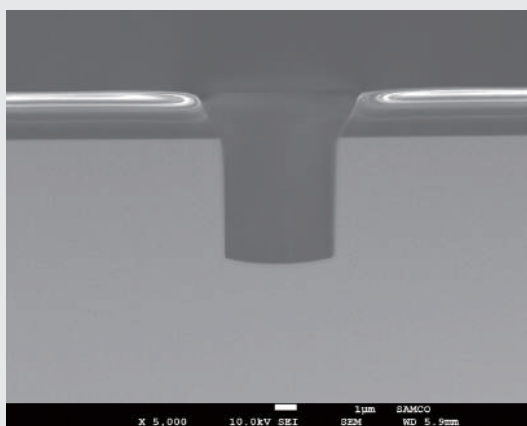


Figure 4. SEM image of high rate ($2 \mu\text{m} / \text{min}$) vertical mesa etch of GaAs DBR VCSEL.

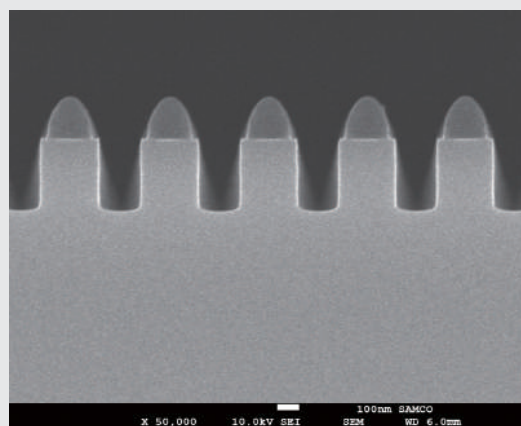


Figure 5. SEM image of grating etch of GaAs HCG-VCSEL.

Conclusion

We introduced our latest GaAs VCSEL dry etch process technology. VCSEL has begun to be installed in more and more smartphones after being adopted by the iPhone X in 2017. Large markets such as LiDAR (Light Detection and Raging) and OCT (Optical Coherence Tomography) are also expected to have an increasing demand for VCSEL. Samco provides to our customers not only dry etching equipment but also the latest process technology. We will continue to contribute to the widespread adoption of VCSELs and the development of this field.

References

1) High-Contrast Grating VCSELs; Connie J. Chang-Hasnain et al. IEEE JOURNAL OF SELECTED TOPICS IN QUANTUM ELECTRONICS, VOL. 15, NO.3, MAY/JUNE 2009



40 Years' Experience in Thin Film Technology

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