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deposition etching surface treatment

New Approach for Trench-Type SiC MOSFET

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Introduction

Compared to the mainstream semiconductor Si, the wide bandgap semiconductor 4H-SiC has excellent material qualities including higher electrical breakdown strength and higher thermal conductivity. Therefore, 4H-SiC has been studied in recent years as a new material to improve miniaturization and energy saving in power devices. Currently, it is being developed not only for device fabrication but also for practical applications in the automotive and power supply industries. SiC MOSFETs (Metal Oxide Semiconductor Field Effect Transistors) are one example of commonly used 4H-SiC power devices that surpass Si power devices in terms of high voltage endurance, low on-resistance, and high-speed switching. Trench type SiC MOSFETs are being developed and have shown that they are capable of achieving a reduced on-resistance, which is highly demanded in current devices. We have been developing a trench etching process using plasma dry etching and deposition of the gate insulator using ALD (Atomic Layer Deposition) and PECVD (Plasma Enhanced Chemical Vapor Deposition). These processes are required for manufacturing trench type SiC MOSFETs. In this paper, we will highlight the SiC trench etching and gate insulator deposition results.

SiC Trench Etching Result

In SiC trench etching, it is vital to achieving a high SiC etch rate and high etch selectivity (SiC/SiO2), while at the same time controlling the sidewall smoothness and etching shape (rounded trench corner and perpendicular sidewall). Four-inch and six-inch wafers are currently the mainstream substrates for 4H-SiC devices. The ICP etching systems we developed are the Samco Model RIE-400iP/iPC for 4-inch wafers and RIE-800iP/iPC for 6-inch wafers. These ICP etching systems can obtain a SiC etching rate of 450 nm/min or more, etch selectivity of 5 or more and etching depth uniformity of ±3% or less. We have also been able to attain the desired etching feature shape (perpendicular sidewall with no micro-trench). The SiC trench etching result using the RIE-800iP is shown in Fig. 1. There is a problem with the electric field tending to concentrate on the bottom corner of the trench in the gate insulator under high device bias. This induces an insulator breakdown at the trench bottom. Thus, the shape of the trench bottom is generally rounded by annealing at about 1500ˆ after etching. We developed a new trench etching process that has rounded corners in the trench bottom without annealing. This etching result is shown in Fig. 2. We are now able to optimize the etching conditions and adjust the roundness of the trench bottom in accordance with a customer's specified trench width and mask thickness.

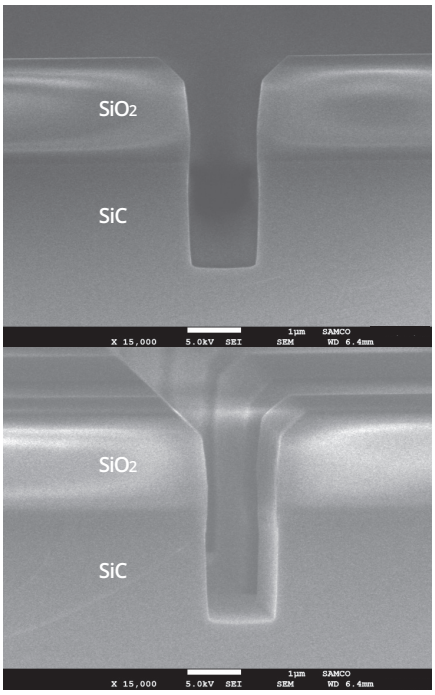
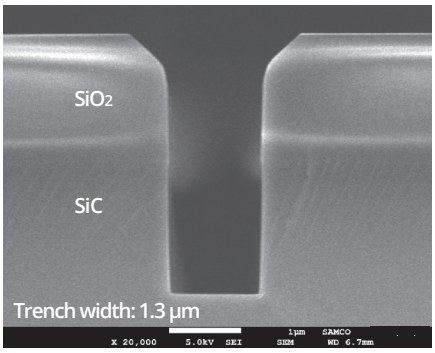
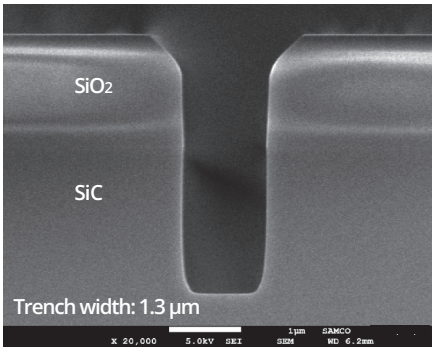


Figure 1. SiC trench etch result using RIE-800iP

Etch depth : 1.98 µm
Etch rate : 464 nm/min
Etch selectivity : 5.5 (SiC/SiO2)



(a) Normal etching process
Etch depth : 1.9 µm



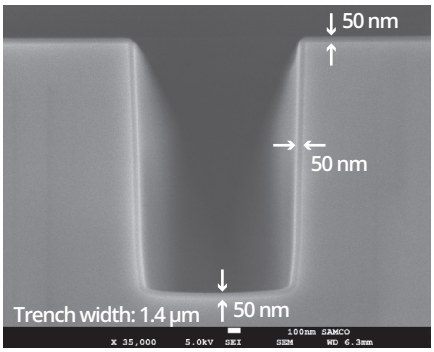
(b) New etching process
Etch depth : 2.1 µm

Figure 2. The result of the new etching process for obtaining rounded trench corner etching of the SiC trench

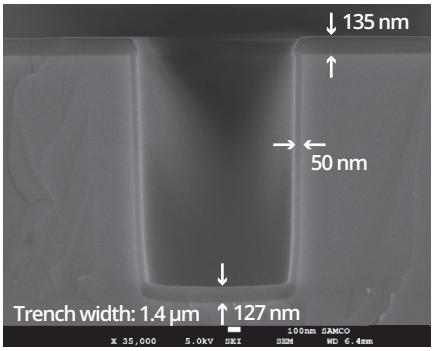
Trench Type SiC Gate Insulator Deposition Results

It is necessary for trench type SiC MOSFET gate insulators to have thin sidewalls for good current flow and thick trench bottoms to increase the breakdown voltage. A gate insulator for SiC power devices is generally formed by SiO2 which is deposited using a combination of ALD and PECVD. The breakdown voltage (BV) and hysteresis in capacitance-voltage (C-V) are higher and smaller, respectively, when SiO2 is deposited using ALD than if PECVD was used. However, SiO2 deposited using ALD is conformal in the trench. On the other hand, with SiO2 deposited using our Cathode-Coupled PECVD, it is possible to increase the thickness of the trench bottom. Moreover, the hysteresis in C-V measurement can be resolved by post deposition annealing.

We tried the deposition of gate insulators using an ALD and PECVD multi-layer, which consisted of SiO2 being deposited on a device using ALD and then depositing another layer on top using PECVD. We fabricated a trench type SiC MOSFET and measured the device characteristics in order to evaluate this gate insulator. We were able to obtain good BV and Vds results using this method. The results of SiO2 deposition in the trench are shown in Fig. 3.



(a) ALD only



(b) ALD and PECVD Multilayer

Figure 3. Deposition of SiO2 film in the SiC trench

Conclusion

We highlighted the results of SiC trench etching and gate insulator deposition, that are necessary to fabricate trench type SiC MOSFETs. There are various steps other than those mentioned above which are required when fabricating trench type SiC MOSFETs. These steps include etching and deposition of SiO2 masks for SiC trench etching and etching of polycrystalline Si gate electrodes and Al electrodes. It is possible to do these additional etching and deposition steps with our process equipment. Samco plans to continue to make significant contributions in the development of the power device field such as 4H-SiC, GaN, and β-Ga2O3 by improving the performance of our process equipment and by accumulating the appropriate process data.